REMARKS

This application has been reviewed in light of the FINAL REJECTION mailed January 3, 2008. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1 – 11 are pending in the application with Claim 1 being in independent form. By the present amendment, Claim 1 is amended. No new subject matter is introduced into the disclosure by way of the present amendment.

Initially, Applicant requests that the title of the invention be amended to recite: "SEMICONDUCTOR DEVICE HAVING SEMICONDUCTOR MEMBER AND MOUNTING MEMBER" as the amended title is believed to be more descriptive of the claimed invention.

I. Rejection of Claims 1 – 10 Under 35 U.S.C. § 102(b)

Claims 1 – 10 are rejected by the Examiner under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,777,383 issued to Stager et al.

Stager et al., discloses a semiconductor chip package with interconnect layers. The Stager et al., package includes a plurality of interconnect pads. Contrary to the Examiner's assertion presented on page 3 of the present Office Action, these interconnect pads, as disclosed in Stager et al., are formed with no clear delineation that would lead one skilled in the art to consider the distribution of interconnect pads to be in two groupings. (See: Stager et al., FIG. 2).

However, even if the interconnect pads as disposed in FIG. 2 were taken to represent two distinct groupings, Stager et al. would still fail to anticipate Applicant's invention, as recited in independent Claim 1. Specifically, Claim 1 recites: "...the interconnect pads forming a plurality of I/O cells including signal terminals, a portion of the I/O cells forming a first group of I/O cells and another portion of the I/O cells forming a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group of I/O cells, the first group of I/O

cells including a plurality of rows of interconnect pads disposed to encircle a center of the mounting member, and the second group of I/O cells including a plurality of rows of interconnect pads disposed to encircle a center of the mounting member..." Applicant submits that Stager et al. neither teaches nor discloses the recited arrangement.

The Examiner continues to insist that FIG. 2 shows two groups of I/O cells. However, the so-called groups in Stager et al. are a construction of the Examiner and not at all taught or even suggested by the disclosure.

Moreover, regardless of any theoretical grouping devised by the Examiner, Stager et al. suffers from the same limitations as described in the background of Applicant's disclosure. Specifically, the Stager et al. arrangement is limited in the number of electrode terminals that can be disposed on the substrate because a limited amount of space is provided between electrode terminals for disposing lead lines. (See: Applicant's FIG. 1 – 3 and associated passages in the background section. For low-density integrated circuit (IC) chips having a small number of electrode terminals, the Stager et al. arrangement may be adequate. However, when dealing with very high-density IC chips, the arrangement taught in Stager et al. would necessitate a significantly larger substrate than is required by Applicant's claimed arrangement.

It is well-settled by the Courts that "[A]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GMBH v. American Hoist and Derrick Company, et al., 730 F.2d 1452, 221 USPQ 481 (Fed. Cir., 1984).

Therefore, as demonstrated above, because Stager et al. does not disclose each and every element recited in the present claims, Applicant respectfully submits that the rejection has been

obviated. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claims 1 - 11 under 35 U.S.C. § 102(b).

II. Rejection of Claim 11 Under 35 U.S.C. § 103(a)

Claim 11 is rejected under 35 U.S.C. § 103(a) over Stager et al., in view of U.S. Patent No. 6,271,478 issued to Horiuchi et al. In response, Applicant respectfully traverses the present rejection with respect to Claim 11 for at least the reasons presented below.

Horiuchi fails to overcome the deficiencies identified above in Stager et al., namely Horiuchi, taken alone or in any proper combination with Stager et al., does not disclose or suggest interconnect pads forming a plurality of I/O cells including signal terminals, a portion of the I/O cells forming a first group of I/O cells and another portion of the I/O cells forming a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group of I/O cells, as recited in amended Claim 1.

Since Claim 11 depends from independent Claim 1, and thus includes all the features recited in that independent claim, Claim 11 is believed to be allowable for at least the reasons presented above. Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claim 11 under 35 U.S.C. § 103(a) over Stager et al. in view of Horiuchi et al.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1 – 11 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

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